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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/741,999	12/22/2000	Richard P. Modelski	P 269864 NOR- 13164BA	7780

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EXAMINER	
MAHMOUDI, HASSAN	
ART UNIT	**PAPER NUMBER**
2165	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/741,999	MODELSKI ET AL.	
	Examiner	Art Unit	
	Tony Mahmoudi	2165	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-5* is/are rejected.

7)☒ Claim(s) *2,6-16 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

SAM RIMELL
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's Request for Continued Examination (RCE) submission filed on 23-December-2004 has been entered. In addition, the "After Final" amendment filed on 04-November-2004 has been entered for the continued examination of this application.

Remarks

2. In response to communications filed on 04-November-2004, independent claims 1 and 5 are amended per applicant's request. Claim 17 had been previously canceled by the applicant, therefore, claims 1-16 and 18 are presently pending in the application, of which, claims 1 and 5 are in independent form.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narad et al (U.S. Patent No. 6,157,955) in view of Hansen et al (U.S. Publication No. 2004/0049663 A1.)

As to claim 1, Narad et al teaches a method for access to bit fields in instruction operands (see Abstract, and see column 11, lines 12-24), the method comprising:

providing bit fields (see column 22, lines 9-15) in a processor executable instruction (see column 3, lines 66-67, and see column 10, lines 32-33), each of the bit fields consisting of a plurality of bits in a plurality of bit positions in the source and target operands (see column 22, lines 9-45, and see TABLE 1);

performing the processor executable instruction utilizing the bit fields in the source and target operands in response to the bit fields (see column 27, lines 4-7, and see column 28, lines 17-24); and

providing, by the performing the processor executable instruction, and in response to the bit fields, direct manipulation of any bits in any bit field (see column 24, lines 50-64, and see column 59, lines 39-50.)

Narad et al does not teach:

direct access to bit fields in instruction operands;

indications of bit fields in source and target operands; and

manipulation of bits in any bit field of the source and target operands.

Hansen et al teaches a method and system with wide operand architecture (see Abstract), in which he teaches:

direct access to bit fields in instruction operands (see paragraphs 61, 128 and 140);

indications of bit fields in source and target operands (see paragraphs 140, 238 and 239); and

manipulation of bits in any bit field of the source and target operands (see paragraphs 8, 63-64 and 89-90.)

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Narad et al to include direct access to bit fields in instruction operands; indications of bit fields in source and target operands; and manipulation of bits in any bit field of the source and target operands.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Narad et al by the teachings of Hansen et al, because including direct access to bit fields in instruction operands; indications of bit fields in source and target operands; and manipulation of bits in any bit field of the source and target operands, would provide the advantage of indicating bit fields and manipulating bit fields in any of the source or destination operands, and storing the results of the bit-manipulations in a third operand, through direct access of the bits in the instruction operands.

As to claim 3, Narad et al as modified, teaches the method further comprising:

transferring the data after modifying and forwarding to an output buffer (see Narad et al, column 9, lines 1-27.)

As to claim 5, Narad et al teaches an apparatus for accessing bit fields in instruction operands (see Abstract, and see column 11, lines 12-24), the apparatus comprising:

at least one memory (see figure 4, see column 7, lines 14-15, and see column 8, lines 12-15);

at least one processor (see column 8, lines 38-39);

a bus interconnecting the at least one memory and the at least one processor (see figure 3, and see column 7, lines 26-31);

wherein one of the at least one processor retrieves bit fields, said bit fields each consisting of a plurality of bits in a plurality of bit positions within the source and target operands (see column 22, lines 9-45, and see column 43, lines 56-60) for a processor executable instruction (see column 3, lines 66-67, and see column 10, lines 32-33), performs the processor executable instruction utilizing the bit fields in source and target operands in response to the bit fields (see column 27, lines 4-7, and see column 28, lines 17-24), and provides, by performance of processor executable instruction, and in response to the bit fields, direct manipulation of any bits in any bit field (see column 24, lines 50-64, and see column 59, lines 39-50.)

for the teaching of "directly accessing bit fields in instruction operands", "indications of bit fields in source and target operands"; and "manipulation of bits in any bit field of

the source and target operands", the applicant is kindly directed to the remarks and discussions made in claim 1 above.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Narad et al (U.S. Patent No. 6,157,955) in view of Hansen et al (U.S. Publication No. 2004/0049663 A1), as applied to claims 1,3 and 5 above, and further in view of Islam et al (U.S. Publication No. 2003/0035430 A1.)

As to claim 4, Narad et al as modified, teaches the method further comprising: processing data (see Narad et al, Abstract.)

Narad et al as modified, still does not teach processing data at a rate of at least 10 Gbs.

Islam et al teaches a programmable network device (see Abstract), in which he teaches processing data at a rate of at least 10 Gbs (see paragraph 43.)

Therefore, it would have been obvious to a person having ordinary skill in the art to have modified Narad et al as modified, to include processing data at a rate of at least 10 Gbs.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Narad et al as modified, by the teaching of Islam et al, because processing data at a rate of at least 10 Gbs, would enhance the processing speed of the data and reduce the processing time and the load on the data networks.

Allowable Subject Matter

6. Claims 2, 6-16 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record, Narad et al (U.S. Patent No. 6,157,955), and Christie et al (U.S. Patent No. 6,157,996), Islam et al (U.S. Publication No. 2003/0035430 A1), Stuttard et al (U.S. Publication No. 2002/0174318 A1), do not disclose, teach, or suggest the claimed limitations of (in combination with all other features in the claim):

transferring data from an input buffer to a packet task manager;

dispatching the data from the packet task manager to an analysis machine;

classifying the data in the analysis machine; and

modifying and forwarding the data in a packet manipulator;

wherein no instruction depends on a preceding instruction because each instruction in a pipeline is executed for a different thread, as recited in dependent claim 2.

The prior art of record, Narad et al (U.S. Patent No. 6,157,955), and Christie et al (U.S. Patent No. 6,157,996), Islam et al (U.S. Publication No. 2003/0035430 A1), Stuttard et al (U.S. Publication No. 2002/0174318 A1), do not disclose, teach, or suggest the claimed limitations of (in combination with all other features in the claim):

an analysis machine having multiple pipelines;

a packet task manager operationally connected to the analysis machine; and,

a packet manipulator operationally connected to the analysis machine, as recited in dependent claim 6.

Claims 7-16 and 18 are objected to because they are dependents from the objected to dependent claim 6.

Response to Arguments

8. Applicant's arguments filed on 04-November-2004 with respect to the rejected claims in view of the cited references have been fully considered but they are moot in view of the new grounds for rejection.

Conclusion

9. Any inquiries concerning this communication or earlier communications from the examiner should be directed to Tony Mahmoudi whose telephone number is (571) 272-4078. The examiner can normally be reached on Mondays-Fridays from 08:00 am to 04:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici, can be reached at (571) 272-4083.

tm

April 18, 2005

SAM RIMELL
PRIMARY EXAMINER